For High-Performance Computing, Data Center, Networking & AI

Fully Hardened HBM2 PHY Solution on TSMC N7

Need lower power? Need more bandwidth? eSilicon has complete high-bandwidth memory solutions from PHY IP, ASIC, interposer and package design through manufacturing.

This data sheet excerpt describes the features and characteristics of the hardened HBM2 PHY solution developed on TSMC N7 technology. For a complete data sheet, contact sales@esilicon.com.

Introduction

High-bandwidth memory achieves higher bandwidth while using less power in a substantially smaller form factor than DDR4 or GDDR5. At 14/16nm, HBM addresses the bandwidth gap with up to 256 GB/s data rate per memory at 2Gbps pin speed. At 7nm, the pin speed increases to 2.4Gbps with bandwidth up to 307GB/s. The HBM2 PHY interface features eight independent channels using a total of 1024 data pins. With support for 2, 4, or 8 HBM2 stacks, the density of signals, coupled with interposer design, requires careful design, thorough timing analysis and validation. eSilicon's HBM2 PHY is a complete, validated hardened IP that is ready for chip integration.

eSilicon's 2.5D/HBM2 is first to production with a comprehensive 2.5D solution that includes eSilicon's HBM2 PHY, interposer and systems in package (SiP) design; volume manufacturing, assembly and test; and complete 2.5D/HBM ecosystem management.

HBM2 SoC Subsystem Benefits

- **Fully hardened** 7nm HBM2 PHY for easy integration
- **Production-ready design available** for licensing: first 7nm product already taped out
- **Fifth generation** of HBM PHYs proven in silicon
- **Interposer design available** for faster time to market
- **Maximum data rate supported** across all timing corners
- **HBM2E** at 3.2Gbps in development
- **Full productization support** available: signal integrity, power integrity and thermal analysis

PHY

The PHY has been developed to the JEDEC JESD 235A specification on TSMC N7 technology.

It supports up to 307.2Gbytes/sec bandwidth with 8x128b channels at 2.4Gbps per I/O.

The PHY is DFI 4.0 compliant with several controller-independent features such as:

- READ/WRITE/CK strobe training
- READ leveling training
- I/O calibration
- Lane repair
- Independent programmable control/status registers (CSRs) via APB or IEEE1500 interface
- MISR test

Integrated I/O

- The I/O supports up to 2.4Gbps DDR operation across a 4mm interposer channel
- Clock speeds up to 1.2Ghz
- Calibrated output current programmable
- Junction operating temperature -40˚C to 125˚C
- Complies with ESD requirements
  - Signals: 70V CDM, 100V HBM, LatchUp ≥ 100mA
  - Power/Ground : 5A (250V) CDM tolerant, 2kV HBM
- Supports flip-chip and 2.5D assembly

PHY Feature	Specification
Data Rate	0.1-2.4Gbps per I/O
Channels	8 independent channels
Self-Refresh	Supported through memory controller
I/O per Channel	212
Channel Bandwidth	Up to 307GB/s
Data I/O	1024 (128 per channel, 8 channels and 16 pseudo channels)
ECC	ECC and parity support in conjunction with the controller. (ECC on DM signals)
Data Byte Invert (DBI)	DBI supported in conjunction with the controller
Data Mask (DM)	DM supported in conjunction with the controller
RAS Support	RAS supported in conjunction with the controller
Cycles/Command	1 cycle (exception is Row Activate at 2 cycles) per JEDEC specification
Interoperability Testing	Supports any third-party DFI 4.0-compliant memory controller vendor
IEEE1500 Support	IEEE1500 ports for direct access to the memory stack and PHY
Impedance Calibration Sharing	Self-contained calibration per PHY instance across all eight channels
Related Signal Pass-Through	Provides ability for signals not related to PHY to be passed through between DRAM stack and ASIC core
Power-Down Modes	IDDQ MODE and dynamic power-down of receivers during WRITE
Temperature Range (Tj)	Function: -40C to 125C 10 years reliability: -10C to 110C
Voltage-Level Target	I/O Voltage: 1.2V +/-5% at uBump Core voltage: 0.75V-5% to 0.85V+10% at uBump

- 1.2V I/O voltage +/-5%
- 0.75V, 0.85V core voltage +10/-5% at uBump

System Integration

Since 2011, eSilicon has been conducting research to develop products and processes that deliver a complete HBM solution. With production 2.5D packaged silicon, eSilicon offers a unique and powerful advantage, delivering the next step of integration, cost reduction, system power management and increasing and integrating system bandwidth by offering a complete HBM solution. It includes IP (PHY, DLL, I/O); Northwest Logic memory controller; ASIC design; SiP design; manufacturing, assembly and test; and complete 2.5D/HBM2 ecosystem management.

Interposer Design

Silicon interposers provide an optimal integration platform:

- Increased signal speed due to shorter interconnects with a smaller form factor
- Reduced parasitics, power, and ESD requirements

This silicon interposer technology platform is based on several enabling process modules and unit process capabilities.

eSilicon interposer design and implementation capabilities:

- Through-silicon via (TSV) system design and wiring analysis
- TSV assembly (chip-to-wafer bonding, temporary bonding/ debonding, etc.)
- Ultra-thin wafer back-grinding and polishing
- Signal and power integrity analysis and IC-to-TSV optimization
- Process design kit (PDK) and EDA flow set-up
- Reliability and failure analysis

Contact & Online Access

Please contact eSilicon at **sales@esilicon.com** for more information, silicon quality results, white papers or complete data sheets.

Resources

Our HBM white paper, ***Start Your HBM/2.5D Design Today,*** co-authored with SK Hynix, Amkor Technology, Northwest Logic and Avery Design Systems, is available on www.esilicon.com.

You may also be interested in our **Advanced ASIC Video Series:**

- *What is High-Bandwidth Memory (HBM2) and 2.5D Packaging?*
- *What is a TCAM?*
- *Where is a TCAM Used in an ASIC?*

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