eSilicon

Enabling Next-Generation Servers, Switches, Routers and 5G
7nm 56G & 112G PAM4 & NRZ DSP SerDes Family

Networking systems are becoming increasingly complex. Meeting the power, performance and density requirements of advanced networking-class ASICs is a significant challenge for system OEMs. Next-generation 12.8, 25.6 and 51.2Tb/s switches and routers demand extreme flexibility in system architecture, greater I/O bandwidth and power scaling to achieve the required performance and density.

Network Challenges

Key challenges facing network architects:

- The number of SerDes lanes is approaching 300
- System power is exploding, sometimes reaching over 400W
- Legacy backplanes have high insertion loss, limiting the maximum throughput

SerDes Joins Our Plug-and-Play 7nm IP Platform

The SerDes family is a critical piece of eSilicon's 7nm IP platform that provides a complete ecosystem of networking-optimized, highly configurable IP. All of the IP in the platform is "plug and play," using the same metal stack, reliability requirements, operating ranges, control interfaces and DFT methodology. This configurability and compatibility results in better performance, higher density and faster time to market.

Enabling Next-Gen 25.6 and 51.2Tb/s Switches, Routers and 800G Systems

At the core of the 7nm IP platform is eSilicon's SerDes technology, which delivers a new level of performance and versatility using a novel DSP-based architecture. Two 7nm PHYs support 56G and 112G NRZ/PAM4 operation to provide the best power efficiency for servers, switches and routers. The architecture delivers unprecedented power efficiency for a true long-reach capability, with hole-free operation down to 1Gb/s. The clocking architecture provides extreme flexibility to support multi-link and multi-rate operations per SerDes lane. A multitude of protocols are supported including a variety of Ethernet standards and Fibre Channel. The architecture also allows further reductions in power consumption for shorter-reach channels.

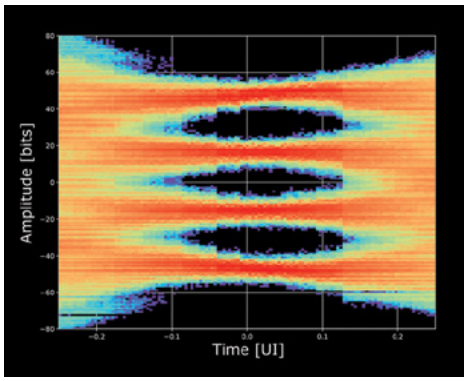
Unique Benefits and Features of eSilicon's 7nm 56G/112G SerDes Family

True Long Reach for the Most Challenging Backplanes

- First-to-market full DSP (Tx and Rx) 56G SerDes in 7nm
- Error-free 56G PAM4 operation over a 30dB backplane without FEC

Easy to Use

- Revolutionary GUI for easy bring-up
- Access non-destructive eye diagrams,



Automatically Generated 7nm 56G DSP SerDes Receive Eye Diagram

SNR and BER, bathtubs, histograms and power measurements from the GUI
- Link monitoring including channel impulse response and error histogram

Unprecedented Power Efficiency

- Best power and reach trade-offs

Flexible & Programmable

- Multiple operational modes support reference and reference-less applications
- Maximum clocking flexibility – Hole-free down to 1Gb/s
- Self-calibrated architecture with optimized power/performance trade-offs
- Multiple IEEE and OIF-standardized protocols, including CPRI, Ethernet and Fibre Channel

Reach Beyond the Rack: an Industry First

Our true long-reach DSP-based SerDes coupled with Samtec's low-loss Twinax Flyover Cable Assembly enables reach beyond the rack: five meters and beyond for data centers and 5G wireless infrastructure. www.samtec.com.

5-Meter Prototype Samtec EBCM Series ExaMAX® Backplane Assembly Featuring Samtec's Low-Loss Twinax Flyover™ Cable

ASIC & SerDes Expertise

Our new SerDes family was developed by a world-class SerDes team with over 12 years of proven experience in networking, including two 28nm silicon-proven 56G SerDes implementations. The new SerDes family leverages the same architecture plus some unique features derived from eSilicon's long-standing experience integrating complex SerDes into bleeding-edge networking ASICs.

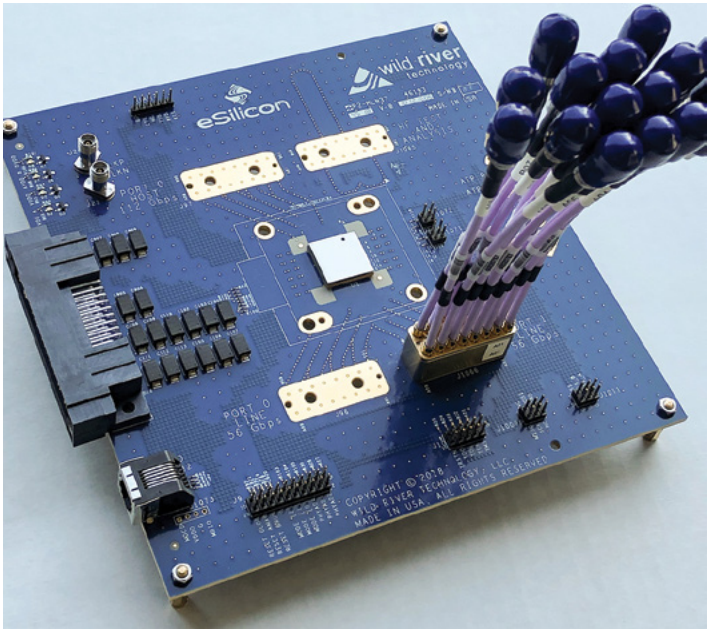
In addition to outstanding performance and versatility, eSilicon's SerDes family provides a new level of user experience for the ASIC design and signal integrity communities. Leveraging a decade of experience integrating complex SerDes into networking ASICs, eSilicon incorporated this unique knowledge into its new 7nm SerDes family. The result is a new-to-the-market, customer-centric SerDes that is easy to integrate and easy to use.

More Information

Additional features and benefits for eSilicon's SerDes family and the rest of the 7nm IP platform are available under NDA.

Check the events page on our website, www.esilicon.com, for information on upcoming live demonstrations around the world. Or you can schedule a demonstration of the 56G SerDes test chip by contacting your eSilicon sales representative directly or via sales@esilicon.com. Demo boards are also available for customer evaluation.

For the latest updates on our 7nm SerDes family, check www.esilicon.com for videos, white papers and blog posts.



eSilicon & Wild River Technology Advanced SerDes test system is available for customer evaluation of eSilicon's 56G PAM4 & NRZ DSP-based 7nm SerDes

QUALITY SYSTEM CERTIFICATION DNV·GL ISO 9001

eSilicon Headquarters
2130 Gold Street, Suite 100
San Jose, CA 95002
1-408-635-6300
www.esilicon.com
https://star.esilicon.com
sales@esilicon.com