Expand System Performance with HBM2: 28/16/14/7nm Hardened HBM2 PHY Solutions for Samsung & TSMC

Need lower power? Need more bandwidth? eSilicon has complete high-bandwidth memory solutions from PHY IP, ASIC, interposer and package design through manufacturing. Take advantage of HBM2 integrated with 2.5D technology to address your power and bandwidth requirements.

This data sheet excerpt describes the features and characteristics of eSilicon's hardened HBM2 PHY solutions on 28/16/14/7nm technologies.

For full-length HBM2 PHY data sheets, contact sales@esilicon.com.

Introduction

With the increasing number of Internet-connected consumer devices, manufacturing systems, business tools, customer service appliances, medical equipment, agricultural sensors, and other devices, the difference between required and available bandwidth will become huge. eSilicon has been studying and refining methods to help close this gap since 2011.

High-bandwidth memory achieves higher bandwidth while using less power in a substantially smaller form factor than DDR4, GDDR5 or hybrid memory cube (HMC).

At 14/16nm, HBM addresses the bandwidth gap with up to 256 GB/s data rate per memory at 2Gbps pin speed.

At 7nm, the pin speed increases to 2.4Gbps and addresses the bandwidth gap with up to 1228 Gbytes/sec data rate with four HBM2 stacks in a package.

HBM has eight independent channels using a total of 1024 input and output pins. This density of signals, coupled with interposer design, requires careful design and thorough timing analysis.

eSilicon's 2.5D/HBM experience includes IP and systems in package (SiP) design; volume manufacturing, assembly and test; and complete 2.5D/HBM ecosystem management.

System Integration

Since 2011, eSilicon has been conducting research to develop products and processes that deliver a complete HBM solution. eSilicon offers a unique and powerful advantage, delivering the next step in integration, cost reduction, and system power management while increasing and integrating system bandwidth via HBM.

Our end-to-end HBM solution includes 2.5D ecosystem management, the PHY, ASIC design, SiP design, manufacturing, assembly and test. Through our partnership with Northwest Logic, we offer a complete HBM interface including both the controller and the PHY, which is silicon validated in an integrated system that includes the interposer and DRAM stack.

HBM SoC Subsystem Benefits:

- **Plug & play:** with hard macro and built-in clock control there's no lengthy timing closure and physical design
- **Custom design** for optimized timing and area
- Rich set of **built-in features**
- **Flexible**: minimum dependence on controller features
- **Signal integrity:** custom routing scheme used on interposer to significantly minimize crosstalk and skew
- **Maximum timing margin:** PHY includes training, calibration and VREF programmability features
- **DFI 4.0 and IEEE1500 compliant**
- **APB interface** enables CPU override of built-in training, repair and calibration

PHY Features

PHY Feature	Specification
Data Rate	0.5-2.4Gbps per I/O
Channels	8 independent channels
Self-Refresh	Feature included
I/O per Channel	212
Channel Bandwidth	Up to 307 GB/s
Data I/O	128/channel, 1024/HBM interface including pseudo channel
ECC	ECC and parity support in conjunction with the controller. (ECC on DM signals)
Data Byte Invert (DBI)	DBI supported in conjunction with the controller
Data Mask (DM)	DM supported in conjunction with the controller
RAS Support	RAS supported in conjunction with the controller
Cycles/Command	1 cycle (exception is Row Activate at 2 cycles) per JEDEC specification
Interoperability Testing	Supports any third-party DFI 4.0-compliant memory controller vendor
IEEE1500 Support	Separate IEEE1500 port for direct access to the memory stack and PHY
Impedance Calibration Sharing	Self-contained calibration per PHY instance across all eight channels
Related Signal Pass-Through	Provides ability for signals not related to PHY to be passed through
Power-Down Modes	IDDQ MODE and dynamic power-down of receivers during WRITE
Temperature Range (Tj)	-40C to 125C

PHY

The HBM2 PHY has been developed to JEDEC JESD235A specification. It has been developed on 28/16/14/7nm.

At 7nm, the PHY supports up to 307Gbytes/sec bandwidth with 8x128b channels at 2.4Gbps per I/O.

The PHY is DFI 4.0 compliant with several controller-independent features such as:

- READ/WRITE/CK strobe training
- READ leveling training
- I/O calibration
- Lane repair
- Independent programmable control/status registers (CSRs) via APB or IEEE1500 interface
- MISR test
- The PHY may be integrated with any controller

Integrated I/O

At 7nm, the I/O supports up to 2.4Gbps DDR operation across a 4mm interposer channel.

- Clock speeds up to 1.2Ghz
- Calibrated output current programmable
- Junction operating temperature -40˚C to 125˚C
- Supports flip-chip assembled SoC device, I/O interfaces to a micro-bump technology

Interposer Design

Silicon interposers provide an optimal integration platform:

- Excellent thermal expansion matching
- Increased signal speed due to shorter interconnects with a smaller form factor
- Reduced RLC parasitics, power and ESD requirements

This silicon interposer technology platform is based on several enabling process modules and unit process capabilities. eSilicon can develop your customized interposers.

eSilicon interposer design and implementation capabilities:

- Through-silicon via (TSV) system design and wiring analysis
- TSV assembly (chip-to-wafer bonding, temporary bonding/debonding, etc.)
- Ultra-thin wafer back-grinding and polishing
- Signal and power integrity analysis and IC-to-TSV optimization
- Process design kit (PDK) and EDA flow set-up
- Reliability and failure analysis

Contact

Please contact eSilicon at **sales@esilicon.com** for more information, silicon quality results, white papers or complete data sheets.

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