TCAM | BCAM

Ternary CAM Compilers

Unlike pre-defined, packaged component products, silicon-proven, low-power ternary CAM compilers let you choose and compile features that fit your design's unique needs to optimize power, performance or area using our patented features. Available from 7nm to 180nm, our TCAM compilers are optimized to meet IDM and leading foundry processes.

When flexibility is everything, eFlexCAM TCAM compilers deliver up to 75 percent power reduction, simply keeping it small and fast.

When Flexibility is Everything

As the demand for digital content explodes, so does the demand for network performance. This has driven the need for processing packets at wire speed.

Memory processing tends to be the bottleneck in network performance. If memory cannot keep up with increasingly fast processors, the processors have to wait, stalling the system. Specialty memories address the problem in a variety of ways. Ternary content-addressable memories (TCAMs) are unique — they search an entire memory database in one cycle. eSilicon's 7nm TCAMs can provide up to 1.8 billion search results in one second (GSPS), worst case.

Silicon-Proven CAMs from 7nm to 180nm

eSilicon has delivered embedded TCAMs to networking customers since 2000, helping them meet the demand for wire-speed packet processing, access control lists and other requirements of high-bandwidth delivery.

eSilicon offers a broad range of silicon-proven,* feature-rich, high-performance, high-density, power-optimized embedded ternary CAM compilers. Our eFlexCAM™ compilers provide high-efficiency, cost-effective solutions for applications such as network search engines, cache for network processors, QoS services, classifications, Ethernet, ATM switches and other diverse networking applications. Search speeds for the 7nm TCAM exceed 1.8 GSPS under worst case operating conditions, and up to 2.5 GSPS under typical operating conditions.

In addition to a full set of standard features, our ternary CAM compilers provide a comprehensive set of user-selectable features that are chosen at compile time. You can choose just the features that you need for a specific application to optimize power, performance or area (PPA).

eFlexCAM CAM designs are available in 7nm to 180nm geometries, optimized to meet challenging PPA requirements of IDM and leading foundry processes. We can supply ternary CAM instances or compilers to fit the number of instances required.

Standard Features

- Multiple architectures available in 7nm, 10nm, 14nm, 16nm, 28nm, 40nm, 65nm, 90nm, 130nm and 180nm
- Flexible selection of width and depth
- Up to 160Kb compiled, 40Mb cascading table size
- Up to 1K entries and up to 160 bits per word
- Easily cascadable to increase search depth without degradation in performance
- Single-cycle search, read and write operations
- Smart Power Management
- Fast cycle and access time: the 7nm TCAM delivers 1.8 GSPS worst case and up to 2.5 GSPS under typical conditions
- Valid-bit, global and local valid-bit reset
- Match-in and match-out flag for each entry
- Flexible masking (bit/group/global)
- Hand-crafted layout for high density and performance

User-Selectable Features

Ternary CAM compilers include many user-selectable features, such as:

- Priority encoder
- Redundancy
- Bit-write

Product Highlights

Flexibility

In contrast to pre-defined, packaged component TCAM products, eSilicon's eFlexCAM compiler lets you choose and compile the features you need to meet your design's specific requirements. This effective integration method, combined with full-custom, pitch-matched floor-planning and layout for each basic cell, results in a highly compact embedded ternary CAM.

Efficient Power Management

Smart Power Management (SPM) architecture allows you to reduce power consumption by up to 75 percent for low-power applications. In the search operation, simply select a single table in Multi-Table Partition (MTP) mode, or a vertical segmented block of the TCAM array in Multi-Width Search (MWS) mode. The remaining unselected portions of the TCAM array will not be activated during the search operation to save power.

The four-quadrant architecture allows you to turn on only one quadrant at a time for searching, reducing peak current significantly. A low-power version of ternary CAM employs strategies to reduce voltage swing of the Hitline and further reduce power required for search operations.

Features

Partial Pipelined Option (PPO)

The array is vertically partitioned into a primary and secondary partition and only entries that match in the primary partition will enable searches of those particular entries on the next clock cycle in the secondary partition. One cycle latency is introduced and throughput is not affected while reducing power as much as 60 percent depending on the number of entries matching in the primary partition.

Patented Duo CAM

The TCAM array is vertically divided into two independent arrays that share a common periphery for reading and writing. Each array has its own match key and match-out flags for each entry. Up to a 30 percent reduction in area and leakage is realized using this feature.

Two-Cycle Read/Write Option

The read/write circuitry is optimized for reduced performance thus realizing ~9 percent reduction in area and leakage power. With this feature two cycles are needed to read or write to and from the array while searches are still performed in one cycle.

Error Correcting Code (ECC)

The patented ECC feature will detect real-time errors on searches including all matching and non-matching entries.

Multi-Width Search Modes (MWS)

eSilicon ternary CAM compilers support the option of multiple-width search mode. You can select from four different search modes: quarter-word (QW), half-word (HW), single-word (SW) and double-word (DW).

Next-Match Mode (NEXTM)

The Next-Match Mode feature allows you to sequentially get Match Addresses of all entries that matched during a search operation. Matches are provided in order of decreasing priority at subsequent clock cycles.

Multi-Table Partition with Addressable Tag Bits (MTP)

MTP allows you to partition the TCAM array into several tables with variable depths using additional tag-bits for table selection. The depth of each table is your choice, as long as each table has the same value for tag-bits. You can select single-table search to save power, or perform full searches across all tables simultaneously.

Look-Aside RAM Buffers (LARB)

With LARB, a RAM block with the same depth as the TCAM array and variable width (user's choice) will be attached to the TCAM instance for area optimization. This option is useful in cache applications, combined with the Write-Back (learning) option.

Dual-Port Search (DPS)

Dual-Port Search allows users to perform two searches in one clock cycle. For this special option, each TCAM cell will have two hit lines and two Match data-in signals.

eSilicon 7FF IP Platform

In addition to our 7FF TCAM compiler, eSilicon offers a complete 7nm FinFET IP platform on TSMC 7FF.

- High-speed single-port (SP) SRAM compiler
- High-speed dual-port (DP) SRAM compiler
- High-speed single-port fast cache (FC) compiler
- High-speed 2-port asynchronous register file (2PARF) compiler
- High-speed pseudo 2-port (P2P) SRAM compiler
- Ultra-high-density (UHD) pseudo 2-port (P2P) SRAM compiler
- High-speed pseudo 4-port (P4P) SRAM compiler
- High-speed pseudo quad-port (PQP) SRAM compiler
- High-speed single-port ternary CAM (SP TCAM) compiler
- 1024-bit HBM2 PHY
- 1.8V oxide 1.8V LVDS I/O library
- 1.8V oxide 1.8V/2.5V/3.3V general-purpose I/O library
- 56G long-reach SerDes

Broad EDA Support

eSilicon memory compilers provide EDA views for leading EDA vendors, helping to ensure seamless integration of our embedded memories into your design flow.

Contact & Online Access

Please contact us at **sales@esilicon.com** for more information, silicon quality results, white papers or data sheets.

All eSilicon IP is available in IP Navigator at **https://star.esilicon.com,** our online IP exploration tool. Navigator provides access to eSilicon's full portfolio of IP products. Memory instances may be generated, analyzed and downloaded. Power, performance, and area (PPA) data is pre-loaded for easy data comparison and analysis.

Resources

Our white papers are available online, including

Why is TCAM Essential for the Cloud?

You may also be interested in our **Advanced ASIC Video Series:**

- *What is High-Bandwidth Memory (HBM2) and 2.5D Packaging?*
- *What is a TCAM?*
- *Where is a TCAM Used in an ASIC?*

QUALITY SYSTEM CERTIFICATION DNV·GL ISO 9001

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