Expand System Performance with High-Bandwidth Memory: HBM Gen2 Hardened PHY Solution on Samsung 14LPP

Is your chip hot? Need more bandwidth? eSilicon has complete high-bandwidth memory solutions from PHY IP, ASIC, interposer and package design through manufacturing.

This data sheet excerpt describes the features and characteristics of the hardened HBM Gen2 PHY solution developed on Samsung 14LPP technology. For a complete data sheet, contact ipbu@esilicon.com.

Introduction
With the increasing number of Internet-connected consumer devices, manufacturing systems, business tools, customer service appliances, medical equipment, agricultural sensors, and other devices, the difference between required and available bandwidth will become huge. eSilicon has been studying and refining methods to help close this gap since 2011.

High-bandwidth memory (HBM) achieves higher bandwidth while using less power in a substantially smaller form factor than DDR4, GDDR5 or hybrid memory cube (HMC). This technology addresses the bandwidth gap with 256 Gbytes/sec data rate per memory with up to four HBM stacks in a package. HBM has eight independent channels using a total of 1024 input and output pins. This density of signals, coupled with interposer design, requires careful design and thorough timing analysis.

eSilicon has designed IP and systems in package (SiP), manufactured, assembled and tested systems that include HBM.

HBM Gen2 SoC Subsystem Benefits:
• Plug & play: with hard macro and built-in clock control there’s no lengthy timing closure and physical design
• Custom design for optimized timing and area
• Rich set of built-in features
• Flexible: minimum dependence on controller features
• Signal integrity: custom routing scheme used on interposer to significantly minimize crosstalk and skew
• Maximum timing margin: PHY includes training, calibration and VREF programmability features
• DFI and IEEE1500 compliant
• APB interface enables CPU override of built-in training, repair and calibration

PHY
The PHY has been developed to JEDEC JESD 235B specification version 2.02. It has been developed on Samsung 14LPP technology with support for 13 and 11 metal layer stack configurations.

The PHY supports up to 256Gbytes/sec bandwidth with 8x128b channels at 2Gbps per I/O.

The PHY is DFI 3.1 compliant with several controller-independent features such as:
• READ/WRITE/CK strobe training
• READ leveling training
• I/O calibration
• Lane repair
• Independent programmable control/status registers (CSRs) via APB or IEEE1500 interface
• MISR test
• The PHY may be integrated with any controller
**Integrated I/O**

The I/O supports up to 2Gbps DDR operation across a 4mm interposer channel
- Clock speeds up to 1Ghz
- Calibrated output current programmable (6mA/9mA/12mA/15mA/18mA)
- Junction operating temperature -40˚C to 125˚C
- ESD requirements: 50V CDM-tolerant, 100V HBM-tolerant
- Supports flip-chip assembled SoC device, I/O interfaces to a micro-bump technology
- 1.2V I/O voltage +/-5%
- 0.8V core voltage +/-10%

**System Integration**

For the past five years, eSilicon has been conducting research to develop products and processes that deliver a complete HBM solution. eSilicon offers a unique and powerful advantage, delivering the next step of integration, cost reduction, system power management and increasing and integrating system bandwidth by offering a complete HBM solution. It includes IP (PHY, DLL, I/O), ASIC design, SiP design, manufacturing, assembly and test.

**Interposer Design**

Silicon interposers provide an optimal integration platform:
- Excellent thermal expansion matching
- Increased signal speed due to shorter interconnects with a smaller form factor
- Reduced RLC parasitics, power, and ESD requirements

This silicon interposer technology platform is based on several enabling process modules and unit process capabilities. eSilicon can develop your customized interposers.

eSilicon interposer design and implementation capabilities:
- Through-silicon via (TSV) system design and wiring analysis
- TSV assembly (chip-to-wafer bonding, temporary bonding/dебonding, etc.)
- Ultra-thin wafer back-grinding and polishing
- Signal and power integrity analysis and IC-to-TSV optimization
- Process design kit (PDK) and EDA flow set-up
- Reliability and failure analysis

**Contact**

Please contact eSilicon at ipbu@esilicon.com for more information, silicon quality results, white papers or complete data sheets.

Our newest HBM white paper, co-authored with SK Hynix, Amkor Technology, Northwest Logic and Avery Design Systems, is available online: [Start Your HBM/2.5D Design Today](#).