Expand System Performance with High-Bandwidth Memory: HBM2 Hardened PHY Solution on Samsung 14LPP

Need more bandwidth? Need lower power? eSilicon and its 2.5D ecosystem have complete, silicon-proven high-bandwidth memory solutions: HBM2 PHY IP, ASIC, interposer & 2.5D package design, test & reliability and volume production.

This data sheet excerpt describes the features and characteristics of the hardened HBM2 PHY solution developed on Samsung 14LPP technology. For a complete data sheet, contact sales@esilicon.com.

Introduction

With the increasing number of Internet-connected consumer devices, manufacturing systems, business tools, customer service appliances, medical equipment, agricultural sensors, and other devices, the difference between required and available bandwidth is becoming huge. eSilicon has been studying and refining methods to help close this gap since 2011.

High-bandwidth memory (HBM) achieves higher bandwidth while using less power in a substantially smaller form factor than DDR4, GDDR5 or hybrid memory cube (HMC). This technology addresses the bandwidth gap with 1,024 Gbytes/sec data rate with up to four HBM stacks in a package. HBM has eight independent channels using a total of 1024 input and output pins. This density of signals, coupled with interposer design, requires careful design and thorough timing analysis.

eSilicon has designed IP and systems in package (SiP), manufactured, assembled and tested systems that include HBM and HBM2 since 2011.

System Integration

Since 2011, eSilicon has been conducting research to develop products and processes that deliver a complete HBM solution. eSilicon offers a unique and powerful advantage, delivering the next step of integration, cost reduction, system power management and increasing and integrating system bandwidth by offering a complete HBM solution. It includes IP (PHY, DLL, I/O), ASIC design, SiP design, manufacturing, assembly and test.

HBM2 SoC Subsystem Benefits:

- **Plug & play:** with hard macro and built-in clock control there's no lengthy timing closure and physical design
- **Custom design** for optimized timing and area
- Rich set of **built-in features**
- **Flexible**: minimum dependence on controller features
- **Signal integrity:** custom routing scheme used on interposer to significantly minimize crosstalk and skew
- **Maximum timing margin:** PHY includes training, calibration and VREF programmability features
- **DFI 4.0 and IEEE1500 compliant**
- **APB interface** enables CPU override of built-in training, repair and calibration

PHY

The PHY has been developed to JEDEC JESD 235A specification. It has been developed on Samsung 14LPP technology with support for 13 and 11 metal layer stack configurations.

The PHY supports up to 256Gbytes/sec bandwidth with 8x128b channels at 2Gbps per I/O.

PHY Feature	Specification
Data Rate	0.5-2Gbps per I/O
Channels	8 independent channels
Self-Refresh	Feature included
I/O per Channel	212
Channel Density	Up to 32Gbits
Data I/O	128/channel, 1024/HBM interface including pseudo channel
ECC	ECC and parity support in conjunction with the controller. (ECC on DM signals)
Data Byte Invert (DBI)	DBI supported in conjunction with the controller
Data Mask (DM)	DM supported in conjunction with the controller
RAS Support	RAS supported in conjunction with the controller
Cycles/Command	1 cycle (exception is Row Activate at 2 cycles) per JEDEC specification
Interoperability Testing	Supports any third-party DFI 4.0-compliant memory controller vendor
IEEE 1500 Support	Separate IEEE1500 port for direct access to the memory stack and PHY
Impedance Calibration Sharing	Self-contained calibration per PHY instance across all eight channels
Related Signal Pass-Through	Provides ability for signals not related to PHY to be passed thru
Power-Down Modes	IDDQ MODE and dynamic power-down of receivers during WRITE
Temperature Range (Tj)	-40C to 125C
Voltage Level Target	VDD (logic supply) at circuit: 0.76V -> 0.935V I/O supply voltage – at package BGA 1.2V (+/-5%)

The PHY is DFI 4.0 compliant with several controller-independent features such as:

- READ/WRITE/CK strobe training
- READ leveling training
- I/O calibration
- Lane repair
- Independent programmable control/status registers (CSRs) via APB or IEEE1500 interface
- MISR test
- The PHY may be integrated with any controller

Integrated I/O

The I/O supports up to 2Gbps DDR operation across a 4mm interposer channel

- Clock speeds up to 1Ghz
- Calibrated output current programmable (6mA/9mA/12mA/15mA/18mA)
- Junction operating temperature -40˚C to 125˚C
- Supports flip-chip assembled SoC device, I/O interfaces to a micro-bump technology
- 1.2V I/O voltage +/-5%
- 0.8V core voltage +/-10%

Interposer Design

Silicon interposers provide an optimal integration platform:

- Excellent thermal expansion matching
- Increased signal speed due to shorter interconnects with a smaller form factor
- Reduced RLC parasitics, power, and ESD requirements

This silicon interposer technology platform is based on several enabling process modules and unit process capabilities. eSilicon can develop your customized interposers.

eSilicon interposer design and implementation capabilities:

- Through-silicon via (TSV) system design and wiring analysis
- TSV assembly (chip-to-wafer bonding, temporary bonding/debonding, etc.)
- Ultra-thin wafer back-grinding and polishing
- Signal and power integrity analysis and IC-to-TSV optimization
- Process design kit (PDK) and EDA flow set-up
- Reliability and failure analysis

Contact

Please contact eSilicon at sales@esilicon.com for more information, silicon quality results, white papers or complete data sheets.

eSilicon Headquarters
2130 Gold Street, Suite 100
San Jose, CA 95002
1-408-635-6300
www.esilicon.com
https://star.esilicon.com
sales@esilicon.com

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